Abstract of the Disclosure:

The semiconductor structure has an interconnect that is isolated by a cavity from an underlying insulating layer on a support. The fabrication method provides for the interconnect firstly to be patterned on a double layer and to be provided with an insulating covering. Then, an opening is etched into the insulating covering, and the lower conductive layer is selectively removed. As a result, one the one hand, low-capacitance wiring can be fabricated and, on the other hand, this enables MOS transistors to be programmed in a simple manner.

WHS:tg - 1999P1192F//1/30/2000